Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	36	(reexecut$9 re-execut$9) near9 ((out adj order$5) hazard$5)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/17 15:11
L2	739	(712/23).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/17 14:24
L3	277	(712/233).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/17 14:24
L4	49326	out adj order$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/17 14:27
L5	239	2 and 4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/17 14:25
L6	44	3 and 4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/17 14:26
L7	154	(load adj instruction$3) near3 branch$5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/17 14:27
L8	50	((out adj order$3) out-of-order$5) near3 load adj instruction$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/17 14:28

L9	468	(712/225).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/17 14:28
L10	11	9 and 8	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/17 14:40
L11	425	(712/216).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/17 14:40
L12	12	8 and 11	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/17 14:40
L13	24	(performance$3 near5 penalty near9 improv$5) and "712"/$.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/17 15:16
L14	28	(performance$3 near5 improv$5 near3 significant$6 near8 processor$5) and "712"/$.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/17 15:17
L15	143	(performance$3 near5 improv$5 near3 significant$6 near8 processor$5)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/17 15:17
L16	2	("6725358").PN.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/17 15:19
L20	206	(load adj instruction$5) near ((subsequen$6 follow following) adj load adj instruction$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/17 15:25

S1	4	(("5913048") or ("6360314")).PN.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/17 14:18
S2	302	glew.in.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/16 17:12
S3	65	glew.in. and "712"/$.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/16 15:12
S4	2	("5951670").PN.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/16 15:32
S5	2	("6725358").PN.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/17 15:19
S6	111	(re-execut$6 reexecut$6) near9 (load adj instruction$5)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/16 17:28
S7	2	(re-execut$6 reexecut$6) near9 (first adj load adj instruction$5)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/16 17:29
S8	1	(re-execut$6 reexecut$6) near9 (one adj load adj instruction$5)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/16 17:29
S9	1	(re-execut$6 reexecut$6) near9 (preced$5 adj load adj instruction$5)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/16 17:36

S10	260	load near3 add near store$5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/16 17:36
S11	0	(first adj load adj instruction$3) near9 add near9 store$5 near9 (second adj load adj instruction$5)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/16 17:43
S12	1	(first adj load adj instruction$3) with add with store$5 with (second adj load adj instruction$5)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/16 17:47
S13	0	(first adj load adj instruction$3) with (second adj load adj instruction$5) with ('same' near3 target$5)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/16 17:48
S14	0	(first adj load adj instruction$3) with (second adj load adj instruction$5) with ('same' near3 target$5 near3 address$6)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/16 17:48

Google Web Images Groups News Froogle more »

"without re-execution" load instruction supersc Search Advanced Search Preferences

Web Results **1** - **3** of about **4** for **"without re-execution" load instruction superscalar processor**. (**0.45** seco

Tip: Try removing quotes from your search to get more results.

[PDF] DSN'00: Fault Tolerance through Re-Execution in Multiscalar ...
File Format: PDF/Adobe Acrobat - View as HTML
... Each **superscalar processor** looking ahead in its region nds only ... with re-execution than **without re- execution**, we expect ... and the re-execution **instruction** streams ...
greg.bronevetsky.com/Byzantine/Hardware/Techniques/ Fault%20Tolerance%20through%20Re-Execution%20in%20Mult... - Similar pages

[PS] F ault T olerance Through Re-execution in Multiscalar Architecture
File Format: Adobe PostScript - View as Text
... to complete a given program with or **without re-execution** is the ... modifications do not effect the **instruction** cache misses ... had no impact as the **load** values were ...
www.ece.wisc.edu/~wander/papers/multiscalar.pdf.gz - Similar pages

[PDF] A High-Bandwidth **Load**-Store Unit for Single- and Multi- Threaded ...
File Format: PDF/Adobe Acrobat - View as HTML
... not surprising that a wide **superscalar** with decent ... when it becomes the oldest **instruction** in the ... Processors 11 squash and mark the **load without re-execution**. ...
www.cis.upenn.edu/departmental/ reports/documents/MS-CIS-04-09.pdf - Similar pages

In order to show you the most relevant results, we have omitted some entries very similar to the 3 already displayed.
If you like, you can repeat the search with the omitted results included.

Free! Get the Google Toolbar. Download Now - About Toolbar



"without re-execution" load instructi Search

Search within results | Language Tools | Search Tips | Dissatisfied? Help us improve

Google Home - Advertising Programs - Business Solutions - About Google

©2004 Google

Google

Web Images Groups News Froogle more »

"without re-execution" load instruction Search Advanced Search Preferences

Web Results **1** - **5** of about **7** for **"without re-execution" load instruction**. (**0.24** seconds)

Tip: Try removing quotes from your search to get more results.

[PDF] DSN'00: Fault Tolerance through Re-Execution in Multiscalar ...
File Format: PDF/Adobe Acrobat - View as HTML
... required to complete the program with re-execution than **without re- execution**, we expect ... rent execution of the actual and the re-execution **instruction** streams. ...
greg.bronevetsky.com/Byzantine/Hardware/Techniques/ Fault%20Tolerance%20through%20Re-Execution%20in%20Mult... - Similar pages

[PDF] A High-Bandwidth **Load**-Store Unit for Single- and Multi- Threaded ...
File Format: PDF/Adobe Acrobat - View as HTML
... the store data arrives, when it becomes the oldest **instruction** in the ... Single- and Multi- Threaded Processors 11 squash and mark the **load without re-execution**. ...
www.cis.upenn.edu/departmental/ reports/documents/MS-CIS-04-09.pdf - Similar pages

[PS] F ault T olerance Through Re-execution in Multiscalar Architecture
File Format: Adobe PostScript - View as Text
... complete a given program with or **without re-execution** is the ... the actual and re-execution **instruction** streams ... information about committed tasks and **load** v alues ...
www.ece.wisc.edu/~wander/papers/multiscalar.pdf.gz - Similar pages

[PDF] MICROSOFT WORD 97 FOR WINDOWS SAMPLE DISSERATATION:
File Format: PDF/Adobe Acrobat - View as HTML
... of **load**, store, branch, and arithmetic operations. The hexadecimal values on the left represent a supposed address associated with each **instruction** and data ...
www.cise.ufl.edu/research/revcomp/ users/sal/jims/StateHistoryRecordingTechniques.pdf - Similar pages

[PDF] ITRA: Inter-Tier Relationship Architecture for End-to-end QoS
File Format: PDF/Adobe Acrobat
... were already executed (and return their results **without re-execution**). ... and share a dispatcher that provide **load** balancing to ... is true for any **instruction** we can ...
www.kluweronline.com/article.asp?PIPS=5268497&PDF=1 - Similar pages

In order to show you the most relevant results, we have omitted some entries very similar to the 5 already displayed.
If you like, you can repeat the search with the omitted results included.

Free! Get the Google Toolbar. Download Now - About Toolbar

Google Search Web PageRank 3 blocked AutoFill Options

"without re-execution" load instructi Search

Search within results | Language Tools | Search Tips | Dissatisfied? Help us improve

Google Home - Advertising Programs - Business Solutions - About Google

©2004 Google

Google

Web Images Groups News Froogle more »

out-of-order load instruction "without re-execu Search Advanced Search Preferences

Web Results **1** - **1** of about **2** for **out-of-order load instruction "without re-execution"** . (**0.20** seconds)

Tip: Try removing quotes from your search to get more results.

[PDF] A High-Bandwidth **Load**-Store Unit for Single- and Multi- Threaded ...
File Format: PDF/Adobe Acrobat - View as HTML
... when it becomes the oldest **instruction** in the ... re-executes all loads that executed **out of order** with respect any older store or **load**; this heuristic ...
www.cis.upenn.edu/departmental/ reports/documents/MS-CIS-04-09.pdf - Similar pages

In order to show you the most relevant results, we have omitted some entries very similar to the 1 already displayed.
If you like, you can repeat the search with the omitted results included.

Free! Google Desktop Search: Search your own computer.

out-of-order load instruction "withou Search

Search within results | Language Tools | Search Tips | Dissatisfied? Help us improve

Google Home - Advertising Programs - Business Solutions - About Google

©2004 Google

IEEE HOME | SEARCH IEEE | SHOP | WEB ACCOUNT | CONTACT IEEE

Membership Publications/Services Standards Conferences Careers/Jobs

IEEE Xplore® RELEASE 1.8

Welcome
United States Patent and Trademark Office

Help FAQ Terms IEEE Peer Review Quick Links

Welcome to IEEE *Xplore*®
- Home
- What Can I Access?
- Log-out

Tables of Contents
- Journals & Magazines
- Conference Proceedings
- Standards

Search
- By Author
- Basic
- Advanced
- CrossRef

Member Services
- Join IEEE
- Establish IEEE Web Account
- Access the IEEE Member Digital Library

IEEE Enterprise
- Access the IEEE Enterprise File Cabinet

Print Format

Your search matched **65** of **1094442** documents.
A maximum of **500** results are displayed, **15** to a page, sorted by **Relevance Descending** order.

Refine This Search:
You may refine your search by editing the current search expression or enteri new one in the text box.

'load instruction'<and>reexecution<or>re execution Search

☐ Check to search within this result set

Results Key:
JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

1 **Re-execution of distributed programs to detect bugs hidden by raci messages**
Kilgore, R.; Chase, C.;
System Sciences, 1997, Proceedings of the Thirtieth Hawaii International Conference on , Volume: 1 , 7-10 Jan. 1997
Pages:423 - 432 vol.1

[Abstract] [PDF Full-Text (988 KB)] **IEEE CNF**

2 **A characterization of re-execution costs for real-time abort-oriente protocols**
LihChyun Shu;
Real-Time Computing Systems and Applications, 1998. Proceedings. Fifth International Conference on , 27-29 Oct. 1998
Pages:286 - 292

[Abstract] [PDF Full-Text (184 KB)] **IEEE CNF**

3 **Fault tolerance through re-execution in multiscalar architecture**
Rashid, F.; Saluja, K.K.; Ramanathan, P.;
Dependable Systems and Networks, 2000. DSN 2000. Proceedings Internatior Conference on , 25-28 June 2000
Pages:482 - 491

[Abstract] [PDF Full-Text (3440 KB)] **IEEE CNF**

4 **Procedure call duplication: minimization of energy consumption wit constrained error detection latency**
Oh, N.; McCluskey, E.J.;
Defect and Fault Tolerance in VLSI Systems, 2001. Proceedings. 2001 IEEE

International Symposium on , 24-26 Oct. 2001
Pages:182 - 187

[Abstract] [PDF Full-Text (154 KB)] IEEE CNF

5 **Error detection by selective procedure call duplication for low energ consumption**
Oh, N.; McCluskey, E.J.;
Reliability, IEEE Transactions on , Volume: 51 , Issue: 4 , Dec. 2002
Pages:392 - 402

[Abstract] [PDF Full-Text (685 KB)] IEEE JNL

6 **Ditto processor**
Shih-Chang Lai; Shih-Lien Lu; Lai, K.; Jih-Kwon Peir;
Dependable Systems and Networks, 2002. Proceedings. International Confere on , 23-26 June 2002
Pages:525 - 534

[Abstract] [PDF Full-Text (358 KB)] IEEE CNF

7 **Backtracking and re-execution in the automatic debugging of parallelized programs**
Matthews, G.; Hood, R.; Johnson, S.; Leggett, P.;
High Performance Distributed Computing, 2002. HPDC-11 2002. Proceedings. IEEE International Symposium on , 23-26 July 2002
Pages:150 - 160

[Abstract] [PDF Full-Text (321 KB)] IEEE CNF

8 **SSD: an affordable fault tolerant architecture for superscalar proces**
Seongwoo Kim; Somani, A.K.;
Dependable Computing, 2001. Proceedings. 2001 Pacific Rim International Symposium on , 17-19 Dec. 2001
Pages:27 - 34

[Abstract] [PDF Full-Text (768 KB)] IEEE CNF

9 **Handling KDD process iteration by integration of planning and controlling**
Chunnian Liu; Ning Zhong;
Systems, Man, and Cybernetics, 1998. 1998 IEEE International Conference on , Volume: 1 , 11-14 Oct 1998
Pages:411 - 416 vol.1

[Abstract] [PDF Full-Text (508 KB)] IEEE CNF

10 **A framework for event-driven demonstration based on the Java too**
Miura, M.; Tanaka, J.;
Computer Human Interaction, 1998. Proceedings. 3rd Asia Pacific , 15-17 July 1998
Pages:331 - 336

[Abstract] [PDF Full-Text (88 KB)] **IEEE CNF**

11 **Compiler optimization of memory-resident value communication between speculative threads**
Zhai, A.; Colohan, C.B.; Steffan, J.G.; Mowry, T.C.;
Code Generation and Optimization, 2004. CGO 2004. International Symposiur on , 20-24 March 2004
Pages:39 - 50

[Abstract] [PDF Full-Text (384 KB)] **IEEE CNF**

12 **On load latency in low-power caches**
Kim, S.; Vijaykrishnan, N.; Irwin, M.J.; John, L.K.;
Low Power Electronics and Design, 2003. ISLPED '03. Proceedings of the 200: International Symposium on , 25-27 Aug. 2003
Pages:258 - 261

[Abstract] [PDF Full-Text (526 KB)] **IEEE CNF**

13 **The R-LRPD test: speculative parallelization of partially parallel loo**
Dang, F.; Hao Yu; Rauchwerger, L.;
Parallel and Distributed Processing Symposium., Proceedings International, IP 2002, Abstracts and CD-ROM , 15-19 April 2002
Pages:20 - 29

[Abstract] [PDF Full-Text (345 KB)] **IEEE CNF**

14 **Commitment-based interoperation for e-commerce**
Jie Xing; Feng Wan; Rustogi, S.K.; Singh, M.P.;
Autonomous Decentralized Systems, 2001. Proceedings. 5th International Symposium on , 26-28 March 2001
Pages:161 - 168

[Abstract] [PDF Full-Text (548 KB)] **IEEE CNF**

15 **Guiding resource constrained software testing**
Rivers, A.T.; Vouk, M.A.;
Software Reliability Engineering, 1999. Proceedings. 10th International Symp on , 1-4 Nov. 1999
Pages:180 - 188

[Abstract] [PDF Full-Text (212 KB)] **IEEE CNF**

1 2 3 4 5 Next

Copyright © 2004 IEEE — All rights reserved

IEEE HOME | SEARCH IEEE | SHOP | WEB ACCOUNT | CONTACT IEEE

IEEE

Membership Publications/Services Standards Conferences Careers/Jobs

IEEE Xplore® RELEASE 1.8

Welcome
United States Patent and Trademark Office

» Se

Help FAQ Terms IEEE Peer Review Quick Links

Welcome to IEEE *Xplore*®
- Home
- What Can I Access?
- Log-out

Tables of Contents
- Journals & Magazines
- Conference Proceedings
- Standards

Search
- By Author
- Basic
- Advanced
- CrossRef

Member Services
- Join IEEE
- Establish IEEE Web Account
- Access the IEEE Member Digital Library

IEEE Enterprise
- Access the IEEE Enterprise File Cabinet

Your search matched **0** of **1094442** documents.
A maximum of **500** results are displayed, **15** to a page, sorted by **Relevance Descending** order.

Refine This Search:
You may refine your search by editing the current search expression or enteri new one in the text box.

'load instruction'<and>control*<and>'transfer data' Search

☐ Check to search within this result set

Results Key:
JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

Results:
No documents matched your query.

Print Format

Home | Log-out | Journals | Conference Proceedings | Standards | Search by Author | Basic Search | Advanced Search | Join IEEE | Web Account | New this week | OPAC Linking Information | Your Feedback | Technical Support | Email Alerting | No Robots Please | Release Notes | IEEE Online Publications | Help | FAQ | Terms | Back to Top

Copyright © 2004 IEEE — All rights reserved

IEEE HOME | SEARCH IEEE | SHOP | WEB ACCOUNT | CONTACT IEEE

IEEE

Membership Publications/Services Standards Conferences Careers/Jobs

IEEE Xplore® RELEASE 1.8

Welcome
United States Patent and Trademark Office

Help FAQ Terms IEEE Peer Review Quick Links

» Se

Welcome to IEEE Xplore®
- Home
- What Can I Access?
- Log-out

Tables of Contents
- Journals & Magazines
- Conference Proceedings
- Standards

Search
- By Author
- Basic
- Advanced
- CrossRef

Member Services
- Join IEEE
- Establish IEEE Web Account
- Access the IEEE Member Digital Library

IEEE Enterprise
- Access the IEEE Enterprise File Cabinet

Print Format

Your search matched **6** of **1094442** documents.
A maximum of **500** results are displayed, **15** to a page, sorted by **Relevance Descending** order.

Refine This Search:
You may refine your search by editing the current search expression or enteri new one in the text box.

'load instruction'<and>control*<and>data Search

☐ Check to search within this result set

Results Key:
JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

1 **Improving the parallelism and concurrency in decoupled architectu**
John, L.; Radhakrisnan, R.;
Parallel and Distributed Processing, 1996. Eighth IEEE Symposium on , 23-26 1996
Pages:130 - 137

[Abstract] [PDF Full-Text (764 KB)] IEEE CNF

2 **Using incorrect speculation to prefetch data in a concurrent multithreaded processor**
Ying Chen; Sendag, R.; Lija, D.J.;
Parallel and Distributed Processing Symposium, 2003. Proceedings. International , 22-26 April 2003
Pages:9 pp.

[Abstract] [PDF Full-Text (276 KB)] IEEE CNF

3 **Enhancing speedup in network processing applications by exploitin instruction reuse with flow aggregation**
Surendra, G.; Banerjee, S.; Nandy, S.K.;
Design, Automation and Test in Europe Conference and Exhibition, 2003 , 20C
Pages:784 - 789

[Abstract] [PDF Full-Text (KB)] IEEE CNF

4 **Field programmable gate array based three-phase PWM inverter**
Mekhilef, S.; Rahim, N.A.;
Transmission and Distribution Conference and Exhibition 2002: Asia Pacific. IEEE/PES , Volume: 3 , 6-10 Oct. 2002
Pages:1953 - 1958 vol.3

[Abstract] [PDF Full-Text (410 KB)] **IEEE CNF**

5 **Compressing address trace data for cache simulations**
Fox, A.; Grun, T.;
Data Compression Conference, 1997. DCC '97. Proceedings , 25-27 March 19
Pages:439

[Abstract] [PDF Full-Text (60 KB)] **IEEE CNF**

6 **Characterization of data value unpredictability to improve predictab**
Thomas, R.; Franklin, M.;
Workload Characterization, 2001. WWC-4. 2001 IEEE International Workshop on , 2 Dec. 2001
Pages:65 - 73

[Abstract] [PDF Full-Text (927 KB)] **IEEE CNF**

Home | Log-out | Journals | Conference Proceedings | Standards | Search by Author | Basic Search | Advanced Search | Join IEEE | Web Account | New this week | OPAC Linking Information | Your Feedback | Technical Support | Email Alerting | No Robots Please | Release Notes | IEEE Online Publications | Help | FAQ| Terms | Back to Top

Copyright © 2004 IEEE — All rights reserved

ACM PORTAL
US Patent & Trademark Office

Subscribe (Full Service) Register (Limited Service, Free) Login

Search: The ACM Digital Library The Guide

+"load instruction*" +"without flushing" SEARCH

Nothing Found

Your search for **+"load instruction*" +"without flushing"** did not return any results.

You may want to try an Advanced Search for additional options.

Please review the Quick Tips below or for more information see the Search Tips.

Quick Tips

- Enter your search terms in lower case with a space between the terms.

 sales offices

 You can also enter a full question or concept in plain language.

 Where are the sales offices?

- Capitalize proper nouns to search for specific people, places, or products.

 John Colter, Netscape Navigator

- Enclose a phrase in double quotes to search for that exact phrase.

 "museum of natural history" "museum of modern art"

- Narrow your searches by using a + if a search term must appear on a page.

 museum +art

- Exclude pages by using a - if a search term must not appear on a page.

 museum -Paris

Combine these techniques to create a specific search query. The better your description of the information you want, the more relevant your results will be.

museum +"natural history" dinosaur -Chicago

The ACM Portal is published by the Association for Computing Machinery. Copyright ?2004 ACM, Inc.
Terms of Usage Privacy Policy Code of Ethics Contact Us

Useful downloads: Adobe Acrobat QuickTime Windows Media Player Real Player

PORTAL
US Patent & Trademark Office

Subscribe (Full Service) Register (Limited Service, Free) Login

Search: The ACM Digital Library The Guide

+"load instruction*" +"without reexecuting"

SEARCH

Nothing Found

Your search for **+"load instruction*" +"without reexecuting"** did not return any results.

You may want to try an Advanced Search for additional options.

Please review the Quick Tips below or for more information see the Search Tips.

Quick Tips

- Enter your search terms in lower case with a space between the terms.

  ```
  sales offices
  ```

 You can also enter a full question or concept in plain language.

  ```
  Where are the sales offices?
  ```

- Capitalize proper nouns to search for specific people, places, or products.

  ```
  John Colter, Netscape Navigator
  ```

- Enclose a phrase in double quotes to search for that exact phrase.

  ```
  "museum of natural history" "museum of modern art"
  ```

- Narrow your searches by using a + if a search term must appear on a page.

  ```
  museum +art
  ```

- Exclude pages by using a - if a search term must not appear on a page.

  ```
  museum -Paris
  ```

Combine these techniques to create a specific search query. The better your description of the information you want, the more relevant your results will be.

```
museum +"natural history" dinosaur -Chicago
```

The ACM Portal is published by the Association for Computing Machinery. Copyright ?2004 ACM, Inc.
Terms of Usage Privacy Policy Code of Ethics Contact Us

Useful downloads: Adobe Acrobat QuickTime Windows Media Player Real Player

ACM PORTAL
US Patent & Trademark Office

Subscribe (Full Service) Register (Limited Service, Free) Login

Search: The ACM Digital Library The Guide

+"load instruction*" +"without re-executing" SEARCH

Nothing Found

Your search for **+"load instruction*" +"without re-executing"** did not return any results.

You may want to try an Advanced Search for additional options.

Please review the Quick Tips below or for more information see the Search Tips.

Quick Tips

- Enter your search terms in lower case with a space between the terms.

  ```
  sales offices
  ```

 You can also enter a full question or concept in plain language.

  ```
  Where are the sales offices?
  ```

- Capitalize proper nouns to search for specific people, places, or products.

  ```
  John Colter, Netscape Navigator
  ```

- Enclose a phrase in double quotes to search for that exact phrase.

  ```
  "museum of natural history" "museum of modern art"
  ```

- Narrow your searches by using a + if a search term must appear on a page.

  ```
  museum +art
  ```

- Exclude pages by using a - if a search term must not appear on a page.

  ```
  museum -Paris
  ```

Combine these techniques to create a specific search query. The better your description of the information you want, the more relevant your results will be.

```
museum +"natural history" dinosaur -Chicago
```

The ACM Portal is published by the Association for Computing Machinery. Copyright ?2004 ACM, Inc.
Terms of Usage Privacy Policy Code of Ethics Contact Us

Useful downloads: Adobe Acrobat QuickTime Windows Media Player Real Player

PORTAL
US Patent & Trademark Office

Subscribe (Full Service) Register (Limited Service, Free) Login

Search: The ACM Digital Library The Guide

+"load instruction" +re-execution +reexecution SEARCH

THE ACM DIGITAL LIBRARY

Feedback Report a problem Satisfaction survey

Terms used **load instruction re execution reexecution** Found **17** of **145,831**

Sort results by relevance

Display results expanded form

Save results to a Binder

Search Tips

Open results in a new window

Try an Advanced Search

Try this search in The ACM Guide

Results 1 - 17 of 17

Relevance scale

1 Predictive techniques for aggressive load speculation

Glenn Reinman, Brad Calder

November 1998 **Proceedings of the 31st annual ACM/IEEE international symposium on Microarchitecture**

Full text available: pdf(1.94 MB) Additional Information: full citation, references, citings, index terms

2 On pipelining dynamic instruction scheduling logic

Jared Stark, Mary D. Brown, Yale N. Patt

December 2000 **Proceedings of the 33rd annual ACM/IEEE international symposium on Microarchitecture**

Full text available: pdf(128.82 KB) ps(543.84 KB) Publisher Site Additional Information: full citation, references, citings, index terms

3 Architecture: Scalable selective re-execution for EDGE architectures

Rajagopalan Desikan, Simha Sethumadhavan, Doug Burger, Stephen W. Keckler

October 2004 **Proceedings of the 11th international conference on Architectural support for programming languages and operating systems**

Full text available: pdf(214.38 KB) Additional Information: full citation, abstract, references, index terms

Pipeline flushes are becoming increasingly expensive in modern microprocessors with large instruction windows and deep pipelines. Selective re-execution is a technique that can reduce the penalty of mis-speculations by re-executing only instructions affected by the mis-speculation, instead of all instructions. In this paper we introduce a new selective re-execution mechanism that exploits the properties of a dataflow-like Explicit Data Graph Execution (EDGE) architecture to support efficient mis ...

Keywords: EDGE architectures, load-store dependence prediction, mis-speculation recovery, selective re-execution, selective replay, speculative dataflow machines

4 Unconstrained speculative execution with predicated state buffering

Hideki Ando, Chikako Nakanishi, Tetsuya Hara, Masao Nakaya

May 1995 **ACM SIGARCH Computer Architecture News , Proceedings of the 22nd**

annual international symposium on Computer architecture, Volume 23 Issue 2

Full text available: pdf(1.50 MB) Additional Information: full citation, abstract, references, citings, index terms

Speculative execution is execution of instructions before it is known whether these instructions should be executed. Compiler-based speculative execution has the potential to achieve both a high instruction per cycle rate and high clock rate. Pure compiler-based approaches, however, have greatly limited instruction scheduling due to a limited ability to handle side effects of speculative execution. Significant performance improvement is, thus, difficult in non-numerical applications. This paper ...

5 Sentinel scheduling for VLIW and superscalar processors

Scott A. Mahlke, William Y. Chen, Wen-mei W. Hwu, B. Ramakrishna Rau, Michael S. Schlansker

September 1992 **ACM SIGPLAN Notices , Proceedings of the fifth international conference on Architectural support for programming languages and operating systems**, Volume 27 Issue 9

Full text available: pdf(1.22 MB) Additional Information: full citation, abstract, references, citings, index terms

Speculative execution is an important source of parallelism for VLIW and superscalar processors. A serious challenge with compiler-controlled speculative execution is to accurately detect and report all program execution errors at the time of occurrence. In this paper, a set of architectural features and compile-time scheduling support referred to as sentinel scheduling is introduced. Sentinel scheduling provides an effective framework for compiler-controlled speculative ex ...

6 Classifying load and store instructions for memory renaming

Glenn Reinman, Brad Calder, Dean Tullsen, Gary Tyson, Todd Austin

May 1999 **Proceedings of the 13th international conference on Supercomputing**

Full text available: pdf(1.37 MB) Additional Information: full citation, references, citings, index terms

7 Speculative execution: Enhancing memory level parallelism via recovery-free value prediction

Huiyang Zhou, Thomas M. Conte

June 2003 **Proceedings of the 17th annual international conference on Supercomputing**

Full text available: pdf(302.33 KB) Additional Information: full citation, abstract, references, index terms

The ever-increasing computational power of contemporary microprocessors reduces the execution time spent on arithmetic computations (i.e., the computations not involving slow memory operations such as cache misses) significantly. Therefore, for memory intensive workloads, it becomes more important to overlap multiple cache misses than to overlap slow memory operations with other computations. In this paper, we propose a novel technique to parallelize sequential cache misses, thereby increasing m ...

Keywords: memory disambiguation, memory level parallelism, prefetching, recovery-free value prediction

8 Zero-cycle loads: microarchitecture support for reducing load latency

Todd M. Austin, Gurindar S. Sohi

December 1995 **Proceedings of the 28th annual international symposium on Microarchitecture**

Full text available: pdf(1.35 MB) Additional Information: full citation, references, citings, index terms

9 Streamlining data cache access with fast address calculation

Todd M. Austin, Dionisios N. Pnevmatikatos, Gurindar S. Sohi

May 1995 **ACM SIGARCH Computer Architecture News , Proceedings of the 22nd annual international symposium on Computer architecture**, Volume 23 Issue 2

Full text available: pdf(1.58 MB) Additional Information: full citation, abstract, references, citings, index terms

For many programs, especially integer codes, untolerated load instruction latencies account for a significant portion of total execution time. In this paper, we present the design and evaluation of a fast address generation mechanism capable of eliminating the delays caused by effective address calculation for many loads and stores.Our approach works by predicting early in the pipeline (part of) the effective address of a memory access and using this predicted address to speculatively access the ...

10 Architectural power estimation and optimization: Power-aware issue queue design for speculative instructions

Tali Moreshet, R. Iris Bahar

June 2003 **Proceedings of the 40th conference on Design automation**

Full text available: pdf(157.45 KB) Additional Information: full citation, abstract, references, index terms

Speculatively issued instructions may be particularly sensitive to increases in pipeline depth. Our results indicate that as pipeline depth increases, speculation increases the percentage of issue queue instructions that are waiting to be potentially re-issued in case of a mis-speculation. To compensate, issue queues are larger and thus more power hungry. We propose an alternative design called the *Dual Issue Queue*, that retains pre- and post-issue instructions in separate, smaller queues ...

Keywords: low power design, microarchitecture, speculation

11 Compiler Optimization of Memory-Resident Value Communication Between Speculative Threads

Antonia Zhai, Christopher B. Colohan, J. Gregory Steffan, Todd C. Mowry

March 2004 **Proceedings of the international symposium on Code generation and optimization: feedback-directed and runtime optimization**

Full text available: pdf(257.99 KB) Additional Information: full citation, abstract

Efficient inter-thread value communication is essential for improving performance in Thread-Level Speculation (TLS). Although several mechanisms for improving value communication using hardware support have been proposed, there is relatively little work onexploiting the potential of compiler optimization.Building on recent research on compiler optimization of scalar value communication between speculative threads, we propose compiler techniques for the optimization of memory-resident values.In T ...

12 Compiler controlled value prediction using branch predictor based confidence

Eric Larson, Todd Austin

December 2000 **Proceedings of the 33rd annual ACM/IEEE international symposium on Microarchitecture**

Full text available: pdf(236.58 KB) ps(850.71 KB) Publisher Site Additional Information: full citation, references, index terms

13 Data prefetching by dependence graph precomputation

Murali Annavaram, Jignesh M. Patel, Edward S. Davidson

May 2001 **ACM SIGARCH Computer Architecture News , Proceedings of the 28th annual international symposium on Computer architecture**, Volume 29 Issue 2

Full text available: pdf(909.40 KB) Additional Information: full citation, abstract, references, citings, index terms

Data cache misses reduce the performance of wide-issue processors by stalling the data supply to the processor. Prefetching data by predicting the miss address is one way to tolerate the cache miss latencies. But current applications with irregular access patterns make it difficult to accurately predict the address sufficiently early to mask large cache miss latencies. This paper explores an alternative to predicting prefetch addresses, namely precomputing them. The Dependence Graph Pr ...

14 Enhancing software reliability with speculative threads

Jeffrey Oplinger, Monica S. Lam

October 2002 **Proceedings of the 10th international conference on Architectural support for programming languages and operating systems**, Volume 37 , 36 , 30 Issue 10 , 5 , 5

Full text available: pdf(1.47 MB) Additional Information: full citation, abstract, references, citings

This paper advocates the use of a monitor-and-recover programming paradigm to enhance the reliability of software, and proposes an architectural design that allows software and hardware to cooperate in making this paradigm more efficient and easier to program.We propose that programmers write monitoring functions assuming simple sequential execution semantics. Our architecture speeds up the computation by executing the monitoring functions speculatively in parallel with the main computation. For ...

15 Checkpoint Processing and Recovery: Towards Scalable Large Instruction Window Processors

Haitham Akkary, Ravi Rajwar, Srikanth T. Srinivasan

December 2003 **Proceedings of the 36th Annual IEEE/ACM International Symposium on Microarchitecture**

Full text available: pdf(419.08 KB) Publisher Site Additional Information: full citation, abstract, citings, index terms

Large instruction window processors achieve high performance by exposing large amounts of instruction levelparallelism. However, accessing large hardware structurestypically required to buffer and process such instructionwindow sizes significantly degrade the cycle time. This paper proposes a novel Checkpoint Processing and Recovery(CPR) microarchitecture, and shows how to implement alarge instruction window processor without requiring largestructures thus permitting a high clock frequency.We fo ...

16 Value-based clock gating and operation packing: dynamic strategies for improving processor power and performance

David Brooks, Margaret Martonosi

May 2000 **ACM Transactions on Computer Systems (TOCS)**, Volume 18 Issue 2

Full text available: pdf(210.51 KB) Additional Information: full citation, abstract, references, citings, index terms

The large address space needs of many current applications have pushed processor designs toward 64-bit word widths. Although full 64-bit addresses and operations are indeed sometimes needed, arithmetic operations on much smaller quantities are still more common. In fact, another instruction set trend has been the introduction of instructions geared toward subword operations on 16-bit quantities. For examples, most major

processors now include instruction set support for multimedia operation ...

17 Register integration: a simple and efficient implementation of squash reuse



Amir Roth, Gurindar S. Sohi

December 2000 **Proceedings of the 33rd annual ACM/IEEE international symposium on Microarchitecture**

Full text available: pdf(154.98 KB) ps(573.81 KB) Publisher Site

Additional Information: full citation, references, citings, index terms

Results 1 - 17 of 17

The ACM Portal is published by the Association for Computing Machinery. Copyright ?2004 ACM, Inc.
Terms of Usage Privacy Policy Code of Ethics Contact Us

Useful downloads: Adobe Acrobat QuickTime Windows Media Player Real Player